

UNITED STATES PATENT APPLICATION

FOR

**METHOD AND APPARATUS FOR DISABLING A COMPUTER SYSTEM BUS
UPON DETECTION OF A POWER FAULT**

Inventor:
Joseph A. Bennett

PREPARED BY:

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1026
(408) 720-8300

EXPRESS MAIL CERTIFICATE OF MAILING

"Express Mail" mailing label number EL 617 210 163 US

Date of Deposit December 29, 2000

I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231

Tina Domingo
(Typed or printed name of person mailing paper or fee)
 12-29-2000
(Signature of person mailing paper or fee) Date

**METHOD AND APPARATUS FOR DISABLING A COMPUTER SYSTEM BUS
UPON DETECTION OF A POWER FAULT**

FIELD OF THE INVENTION

The present invention pertains to the field of computer systems. More
5 particularly, this invention pertains to the field of disabling a computer system bus upon
detection of a power fault.

BACKGROUND OF THE INVENTION

Computer system components may communicate one with another by way of a
computer system bus. A computer system may include several busses. A device that
10 couples one bus to another is typically referred to as a bus bridge. Computer system
busses include multiple signal lines, including lines that deliver power to various system
components. If a bus experiences a power fault of some kind, such as a short between a
power line and some other line, that bus will malfunction. A power fault of this type
would likely result in system component malfunction. A bus bridge device coupled to the
15 malfunctioning bus may also malfunction, in that it may be exposed to invalid data that
would be passed on to other system components, such as a processor. The end result
would be an entire system failure.

Some current computer systems implement what is often referred to as “hot plug”
slots, where system components mounted on cards may be inserted into slots that are
20 fixed to a main computer system board. The slots are electrically coupled to a bridge
device via a bus. The term “hot plug” is meant to indicate that a card may be inserted or
removed without powering down the system. Some hot plug systems implement power
fault protection schemes whereby if a power fault is detected at one of the slots, power is

removed from that slot. Hot plug power fault implementations have the disadvantage of being relatively expensive to implement due to the extra motherboard and bridge device hardware as well as the software stack that is required to manage a hot plug environment.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be understood more fully from the detailed description given below and from the accompanying drawings of embodiments of the invention which, however, should not be taken to limit the invention to the specific embodiments
5 described, but are for explanation and understanding only.

Figure 1 is a block diagram of a system including a bus bridge device and a power regulator implemented in accordance with one embodiment of the invention.

Figure 2 is a flow diagram of one embodiment of a method for disabling a computer bus upon detection of a power fault.

00000000000000000000000000000000

DETAILED DESCRIPTION

One embodiment of a system for disabling a computer bus upon detection of a power fault includes a bus bridge device coupled to a bus and a power regulator that delivers power to the bus. If the power regulator detects a power fault, then the power 5 regulator asserts a fault signal to the bus bridge device. The power regulator also removes power from the bus. The bus bridge device disconnects an internal logic unit from the bus in response to the assertion of the fault signal. The bus bridge device, in further response to the assertion of the fault signal, alerts the system of the power fault by asserting an interrupt signal.

10 **Figure 1** is a block diagram of a system 100. The system 100 includes a processor 110 coupled to a system logic device 120. The system logic device 120 is also coupled to a graphics controller 130 and a system memory 140. The system logic device 120 is further coupled to a primary peripheral component interconnect (PCI) bus 125. The system logic device 120 allows the processor 110 to communicate with the system 15 memory 140, the graphics controller 130, and the primary PCI bus 125. Similarly, the system logic device 120 allows PCI bus agents to access the system memory 140. The graphics controller 130 may also access the system memory 140 through the system logic device 120. The system logic device 120 may also receive error signals and interrupts from the primary PCI bus 125 and may in turn signal interrupts to the processor 110. The 20 processor 110, the system logic device 120, the graphics controller 130, and the system memory 140 are meant to represent a broad range of processors, system logic devices, and system memory implementations. Embodiments are also possible with system

configurations other than that shown in **Figure 1**, including systems with more than one processor.

The primary PCI bus 125 is further coupled to a PCI-PCI bridge 150. The PCI-PCI bridge 150 couples the primary PCI bus 125 to a secondary PCI bus 155. The 5 secondary PCI bus 155 has coupled to it several PCI devices 170, 180, and 190. These devices may include disk drive controllers or other input/output devices. Other embodiments are possible using other PCI components.

A power regulator 160 delivers power to the secondary PCI bus 155. When the system 100 is first started, the PCI-PCI bridge 150 asserts a power enable signal 157 to 10 the power regulator 160. The power regulator 160 then applies power to the secondary PCI bus 155. If the power regulator 160 detects a short or other power fault condition, the power regulator 160 removes power from the secondary PCI bus 155 and asserts a fault signal 165. The power regulator 160 may detect a fault by detecting an undervoltage condition or an overcurrent condition. The term “power regulator” as used herein is 15 meant to include any device capable of delivering power to a bus or other type of system component interconnect.

The fault signal 165 is received by the PCI-PCI bridge 150. In response to the assertion of the fault signal 165, the PCI-PCI bridge 150 disconnects its internal logic from the secondary PCI bus 155 so that the internal logic of the PCI-PCI bridge 150 will 20 not become corrupted with invalid data from the secondary PCI bus 155. The PCI-PCI bridge 150 also signals an interrupt to the system logic device 120 over the primary PCI bus 125. Other embodiments may include the PCI-PCI bridge 150 asserting an error signal that is delivered to the system logic device 120. Still other embodiments are

possible using any other technique for signaling an error or fault condition, including write transactions to memory that are directed to or visible to one or more processors.

Once the processor 110 is notified of the pending interrupt or error condition, system software can then take steps to schedule a system shutdown or take other steps such as alerting a system administrator of the fault condition.

The PCI-PCI bridge 150 may also deassert the power enable signal 157. The power regulator 160 will not again deliver power to the secondary PCI bus 155 unless the PCI-PCI bridge 150 asserts the power enable signal 157.

In response to the deassertion of the power enable signal 157, the power regulator 160 deasserts the fault signal 165.

Although the busses discussed above in connection with **Figure 1** are PCI busses, other embodiments are possible using other types of busses or system component interconnects. Also, although the system 100 and the corresponding discussion above describe a PCI-PCI bridge device with the ability to receive and react to the fault signal, other embodiments are possible where the fault signal recognition, the power enable signal assertion, or the disconnecting of internal logic capabilities are located in other computer system component types.

Figure 2 is a flow diagram of one embodiment of a method for disabling a computer system bus upon an occurrence of a fault condition. At block 210, power is applied to a bus. If a power fault is detected at block 220, the power is removed from the bus at block 230. At block 240, a fault signal is asserted to a bus bridge device. Other embodiments are possible using other types of system components.

In response to the assertion of the fault signal, at block 250 the bus bridge device disconnects an internal logic unit from the bus. Lastly, at block 260 an interrupt is asserted to alert the system of the fault condition. Other embodiments are possible using other techniques for signaling error conditions or faults.

5 In the foregoing specification the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than in a restrictive
10 sense.

Reference in the specification to "an embodiment," "one embodiment," "some embodiments," or "other embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments, of the invention. The various
15 appearances of "an embodiment," "one embodiment," or "some embodiments" are not necessarily all referring to the same embodiments.